Patent claims

1. Slave circuit which can be connected in series with further slave circuits (1-i) and a master circuit (30) to form a ring structure, having:

(a) a data transmission interface (2) for processing data frames which are received from the master circuit (30),

where the data transmission interface (2) has an external data input (4) for receiving the data frames from the master circuit (30) and a data output (23) for sending data frames to the next series connected slave circuit,

where each data frame contains at least a first data field for an address and a second data field for transmitting user data;

(b) an address register (10) for storing an address,

where the address register (10) has stored, prior to the initialization of the slave circuit by the master circuit (30), a predetermined initialization address (UIA) which is provided for all the slave circuits (1-i) jointly;

(c) a comparator (13) for comparing the address stored in the address register (10) with an address received from the data transmission interface (2) in a data frame,

where the address register (10) stores the data transmitted in the second data field of the data frame as a future address for the slave circuit (1) if the address transmitted in the first data field of the data frame is identical to the predetermined initialization address (UIA);

(d) an indicator register which indicates the initialization of the slave circuit (1) if the address received by the data transmission interface (2) in the

slave circuit (1) is identical to the predetermined initialization address (UIA); and having

(e) an inhibit logic unit (19) which inhibits the data output (23) of the data transmission interface (2) until the indicator register (16) indicates initialization of the slave circuit (1).

2. Slave circuit according to claim 1, characterized in that the data transmission interface (2) has a data output (23) for sending data, an internal data output for sending the data extracted from the received data frame in line with a data transmission protocol to a data processing unit (8), an internal address output for sending the address extracted from the received data frame in line with the data transmission protocol to the data processing unit (8), and a clock signal input (5) for receiving a clock signal.

3. Slave circuit according to claim 5, characterized in that the indicator register (16) is a flipflop which is actuated by the comparator (13).

4. Slave circuit according to one of the preceding claims, characterized in that the data output (23) is at logic high in the inactive state of the data transmission interface (2), and in that the indicator flipflop (16) is at logic high if the slave circuit (1) has not been initialized.

5. Slave circuit according to claim 4, characterized

in that the inhibit logic unit (19) has:
an OR gate (37), whose first input is connected to the external data input (4) of the data transmission interface (2) and whose second input is connected to the indicator flipflop (16), and
an AND gate (38), whose first input is connected to the output of the OR gate (37) and whose second input is connected to the data output (23) of the data transmission interface (2).

6. Slave circuit according to claim 1, characterized
in that the inhibit logic unit (19) has a synchronization flipflop (26) connected downstream of it.

7. Slave circuit according to claim 6, characterized
in that when the slave circuit (1-i) is connected in series with a further slave circuit (1-i+1) the respective output (29) of the synchronization flipflop (26) in a slave circuit (1-i) is connected to the external data input (4) of the further downstream slave circuit (1-i+1).

8. Slave circuit according to claim 7, characterized
in that when the slave circuits (1-i) are connected in series with the master circuit (30) to form a ring structure the external data input (4-1) in the first slave circuit (1-1) is connected to a data output (34) on the master circuit (30), and the output (29-N) of the synchronization flipflop (29-N) in the last slave circuit (1-N) is connected to a data input (36) on the master circuit (30).

9. Slave circuit according to one of the preceding claims,
characterized
in that the slave circuit (1) is an integrated circuit having three connections, namely
a first connection (4), which is connected to the data input of the data transmission interface (2),
a second connection (29), which is connected to the output (27) of the synchronization flipflop (26), and
a third connection (5), which is connected to the clock input of the data transmission interface (2) and to the clock input of the synchronization flipflop (26).

10. Slave circuit according to one of the preceding claims,
characterized
in that the data transmission protocol for processing the transmitted data frames is an HDLC protocol.

11. Method for initializing slave circuits (1) which are connected in series with a master circuit (30) in a ring structure,
where the master circuit (30) successively sends a plurality of initialization data frames, which each contain a common initialization address (UIA) stored in the slave circuits (1-i) and an address which has been assigned by the master circuit (30) for the respective slave circuit (1-i), to the series connected slave circuits (1-i) until the master circuit (30) itself receives an initialization data frame which it has sent,
where a slave circuit (1-i) inhibits forwarding of a data frame to a slave circuit (1-i+1) connected downstream of it until the slave circuit (1-i) is initialized by a received initialization data frame,

where a slave circuit (1-i), upon receiving an initialization data frame, stores the address contained in a data field of the initialization data frame as a future address for itself.